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Design and Implementation of Time-Frequency Taming Algorithm of Rubidium Atomic Clock Based on FPGA

Sun Songfei, Hou Yuanhang, Lv Yiheng, Wang Zhiming, Chen Qun*

Henan Polytechnic, Zhengzhou 450000, China

Corresponding author: Chen Qun , chenqun918@126.com

Absrtact: Synchronously improving the accuracy of time and frequency sources in electronic measurement systems can enhance measurement precision. Fully combining the good long-term stability of 1pps output from satellite navigation receiver and the good terminal stability of rubidium atomic clock, a frequency and time-locked algorithm based on second-order digital phase-locked loop is designed, which integrates frequency taming and time synchronization, and is implemented based on FPGA; The test results show that the algorithm can obtain a better accuracy 1PPS time signal while taming the frequency with good long-term stability external 1pps.

Key words: Rubidium Atomic Clock; Digital Phase Locked Loop; Lpps; Frequency Taming

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Introduction

In the process of electronic measurement, the accuracy of time and frequency sources greatly affects the accuracy of measurement results. Many instruments are equipped with external frequency sources and time/event trigger source input interfaces. In many high-precision measurement scenarios, instruments and equipment need to be connected to high-precision frequency sources such as temperature-controlled crystal oscillators and atomic clocks.

Rubidium atomic clocks offer advantages such as high short-term and long-term stability, high frequency accuracy, and low aging rates, and have been widely used in situations requiring high precision in time and frequency. Although rubidium atomic clocks are stable and accurate, the frequency will always drift and accumulate over time, leading to a drift in both time and frequency; to address this issue, the frequency drift of rubidium atomic clocks can be corrected using pulse signals (1pps) generated by satellite navigation receivers with good long-term stability[1][2][3].

In order to solve this problem, extensive research has been carried out in the industry, such as Lu Xianghong et al. proposed the design of a constant temperature crystal oscillator frequency calibration system based on FPGA [4], Liu Tieqiang et al. proposed the design of a clock taming system based on Beidou timing [5], and Fan Wenjing et al. improved the application of Kalman filter algorithm in clock taming technology [6]. Most of these algorithms and applications focus on taming the frequency of the constant temperature crystal oscillator or atomic clock, overcoming the frequency drift and improving the frequency accuracy. However, in many applications, not only accurate frequency signals are required, but also 1pps (second pulses) are required to characterize accurate time signals [7].

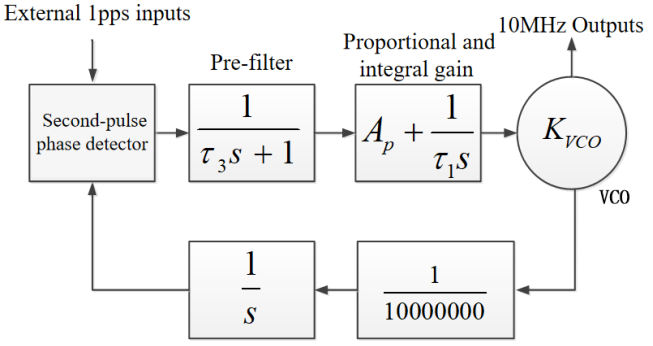
Based on the second-order digital phase-locked loop, the frequency of the rubidium atomic clock is tamed by using an

external 1pps [8]; At the same time, the loop output is more accurate than the external 1pps, and the frequency lock and time lock are completed at the same time. The high-speed FPGA is used as the processor for the implementation of the algorithm, which has the characteristics of fast processing speed, high real-time performance, and good stability [9][10][11].

1.Design of Rubidium atomic clock frequency-locked phase-locked algorithm based on second-order digital phase-locked loop

The block diagram of the phase-locked loop is shown in Figure 1, where the "second pulse phase detector" performs phase detection of the 1pps from the external input and the 1pps generated by the frequency division of the rubidium atomic clock, with a gain of $K_{det} = 1bit / ns$. The loop filter is a digital filter that consists of a pre-filter and a standard programmable proportional-integral (PI) controller. The VCO is the rubidium atomic clock with a frequency of f, which is tuned by voltage, and the parameters adjust the frequency, with a 1pps output sensitivity of $K_{vco} = 0.001ns / bit - s$,or $(1/10^{12})$. The response function of each component of the digital phase-locked loop corresponds to the standard Laplace variable s depicted in the figure.

Figure 1 Block diagram of an external 1pps phase-locked loop



The PI controller is controlled by selecting the appropriate integrator time constant of τ_1 and a stability factor of ζ, τ_1 determines the natural time constant of the PLL τ_n, τ_n represents the step size of the tracking reference phase, while ζ determines the relative rise time and ringing of the PLL based on the step size. A value of ξ also represents the balance between the equivalent noise bandwidth and the peak passband near the natural frequency of the response function. The integration time constant is τ_1, from 2^8 to 2^{22} seconds. The natural time constant is given by $\tau_n = \sqrt{\tau_1 / K_{det} K_{vco}} = \sqrt{(1000s)\tau_1}$. Thus, the natural time constant ranges from 506 seconds to 18 hours. The integral time constant τ_1 determines the natural time constant τ_n, which is the natural time constant describing the loop response.

The stability factor ζ ranges from 0.25 to 4.0. The default value of $\zeta = 1.0$ corresponds to the critical damping response; $\zeta < 1.0$ and $\zeta > 1.0$ correspond to underdamped and overdamped responses, respectively.

Given τ_1 and ζ, the proportional gain of the controller is A_p, as given by equation $A_p = 2\zeta\sqrt{\tau_1 K_{det} K_{vco}} = 2\zeta\sqrt{(0.001s^{-1})\tau_1}$. With the default constant of τ_1 = 65536 seconds and $\zeta = 1.0$, the proportional gain is approximately 0.25. In this case, the instantaneous frequency of the rubidium atomic clock will be adjusted by about 0.25 parts in every measured nanosecond of 10^{12}.

The pre-filter exponentially averages the time labels output from the "second pulse phase detector" before passing the results to the PI controller. The time constant of the pre-filter is τ_3, which is coded as $\tau_n / 6.0$, which is to obtain maximum average benefit while ensuring that the phase-locked loop will be stable. The smoothing effect of the pre-filter greatly reduces the sensitivity of the 1pps phase jitter that occurs between 50ns and 300ns on the external reference 1pps of the digital phase-locked loop. The 1pps output of the GPS/Beidou navigation receiver has a large amount of noise associated with $1/f$; Therefore, a long time constant is required to prevent the rubidium atomic clock from getting too close to this noise. The system provides a natural time constant of up to 18.0 hours, which will allow the rubidium atomic clock to track the 1pps output of the GPS/Beidou navigation receiver on a one-day time scale, while retaining the superior short-term stability of the rubidium clock.

The digital phase-locked loop will approach the following three equations in the case of different ζ .

$$\Delta T(t)=\frac{F_0-\zeta\Delta T(0)/\tau_n}{\sqrt{1-\zeta^2}/\tau_n}e^{\frac{-\zeta t}{\tau_n}}\sin(\sqrt{1-\zeta^2}t/\tau_n)$$
$$+\Delta T(0)e^{\frac{-\zeta t}{\tau_n}}\cos(\sqrt{1-\zeta^2}t/\tau_n) \qquad \text{for } \zeta<1$$

$$\Delta T(t)=t[F_0-\Delta T(0)/\tau_n]e^{\frac{-t}{\tau_n}}+\Delta T(0)e^{\frac{-t}{\tau_n}}$$
$$\text{for } \zeta=1$$

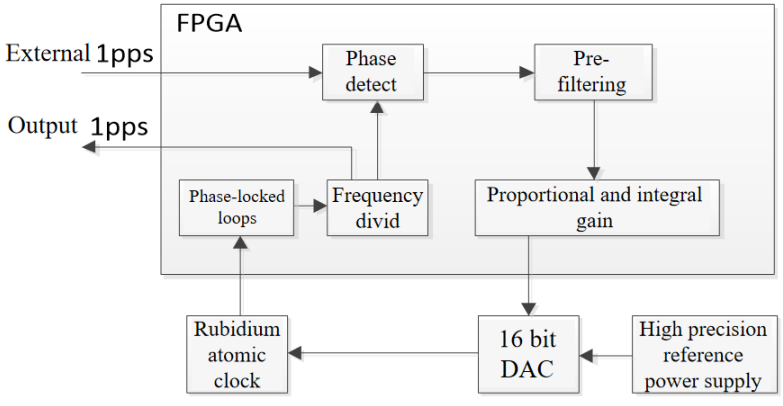
$$\Delta T(t)=\frac{-[F_0-(\zeta+\sqrt{\zeta^2-1})\Delta T(0)/\tau_n]}{2\sqrt{\zeta^2-1}/\tau_n}e^{\frac{-(\zeta+\sqrt{\zeta^2-1})t}{\tau_n}}$$
$$+\frac{[F_0-(\zeta-\sqrt{\zeta^2-1})\Delta T(0)/\tau_n]}{2\sqrt{\zeta^2-1}/\tau_n}e^{\frac{-(\zeta-\sqrt{\zeta^2-1})t}{\tau_n}} \qquad \text{for } \zeta>1$$

$\Delta T(0)$ is the initial phase deviation between the rubidium atomic clock and the reference. F_0 is the frequency difference between the digital phase-locked loop and the reference before it is activated. $\Delta T(t)$ describes the time function when the phase of the rubidium atomic clock reaches the phase of the reference. At the default time constant of $\tau_1 = 65536$ seconds and a stabilization factor of $\zeta = 1.0$, the 1pps output produced by the rubidium atomic clock will be exponentially close to the reference 1pps phase with a time constant of $\tau_n = 8095$ seconds or 2.25 hours.

2.Implementation of Rubidium atomic clock frequency-locked phase-locked algorithm based on second-order digital phase-locked loop

The 10MHz frequency output of the rubidium atomic clock first enters the phase-locked loop inside the FPGA and is doubled to 320MHz, which is used as the master clock for internal counting and processing to improve the accuracy of processing.

Figure 2 Block diagram of time and frequency locking



The first step is 1pps phase calibration. Because the 1pps external 1pps produced by the rubidium atomic clock itself has a large phase difference, after receiving 256 consecutive "good" external 1pps inputs (e.g. the 1pps of subsequent inputs and the first 1pps phase error of less than 2048ns). The 1pps phase produced by the rubidium atomic clock assignment is corrected to the 1pps phase of the last external input. In addition, the current value of the frequency control parameters of the rubidium atomic clock (such as the calibration value at the factory) is used to initialize the integrator in ±2000 units of $\pm 10^{12}$, and the exponential filter after the "second pulse phase detector" is reset to zero.

The second step is frequency and 1pps taming; The frequency is locked to a "good" 1pps input pulse, and a bad "1pps input (the time label of the 1pps input is 1024ns larger than the time label of the previous "good" 1pps input) will be rejected. The frequency parameter f of the frequency control command will be updated with each "good" timestamp result, $\Delta T(n)$, As shown below:

Prefilter:

$$\overline{\Delta T}(n+1)=(1.0-\Delta t/\tau_3)\overline{\Delta T}(n)+(\Delta t/\tau_3)\Delta T(n)$$

Integral term:

$$Int(n+1)=Int(n)-(\overline{\Delta T}(n+1)/\tau_1)K_{det}\Delta t$$

Proportional term:

$$Pro(n+1)=-A_p\overline{\Delta T}(n+1)K_{det}$$

Frequency setting:

$$f(n+1)=Pro(n+1)+Int(n+1)$$

In the above equations, Δt is the time interval between phase comparisons, which is 1 second for this system. The range of the frequency control value f exceeds ±2000 counts. If the new value of f exceeds 2000, it is set to 2000. If the new value of f is less than -2000, it is set to -2000. If the new integral term exceeds 2000, it is set to 2000. If the new integral term is less than -2000, it is set to -2000. This prevents the integrator from diverging when holding a fixed f value for an extended period to align the 1pps output with the 1pps input.

The third step is to control the frequency of the rubidium atomic clock. The output f of the digital filter serves as the frequency control word, which is converted into a voltage signal by a 16-bit high-precision DAC to control the frequency of the rubidium atomic clock, updated once per second. To ensure the precision of the control voltage, the DAC employs a high-precision reference voltage source.[12][13]。

If there are 256 consecutive “bad” 1pps inputs, the PLL will terminate and restart (this may occur if the 1pps input suddenly shifts by more than 1024 ns). The PLL will also terminate and restart if the measurement time tag value of the “good” 1pps input exceeds $\pm 4ns / s * \tau_1$(a situation that may occur if the frequency of the input 1pps deviates from 10^{-9} by several units for an extended period), when the default value of τ_1 is 65536 seconds, if the cumulative phase difference of the "good" 1pps exceeds 262144 nanoseconds, the PLL will restart.

3.Test Results

The test method employed is a comparative test using two identical devices; hence, the measured error represents the relative error between the two devices. The test utilizes a frequency counter, model 53220A. To ensure stable test output results and to create a fixed phase delay between the 1pps outputs of the two devices, a cable delay method is used. This facilitates the setup of the test gate signal. During the test, only the variance and maximum range need to be monitored. The test is set to take a measurement every two seconds, and in the test graphs, one data point corresponds to a time interval of two seconds.

3.1 Performance of the 1pps Output from the Navigation Module

Figure 3: Performance of the 1pps Output from the Navigation Module

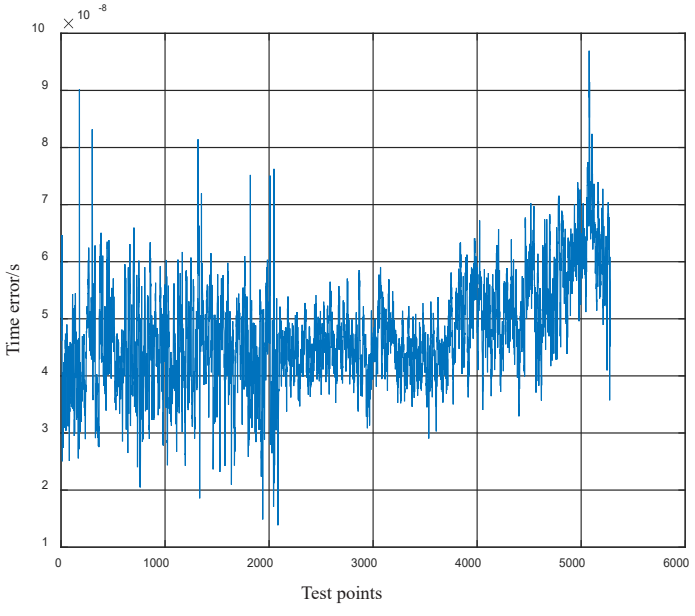


Figure 3 shows the performance of the raw 1pps output from the navigation module. The variance of the time error in the data is 9.09 ns, and the difference between the maximum and minimum values is 83.12 ns. The test data indicates that the error in the original 1pps output from the navigation module is relatively large. This test data is affected by factors such as the environment where the antenna is located and the climatic conditions. However, subsequent tests were also conducted under essentially the same conditions.

3.2 Time Phase Correction and Locking

Figure 4 illustrates the initial phase correction process. During the initial stage, the phase of the 1pps generated by the free-running rubidium atomic clock is corrected using 256 consecutive 1pps inputs with small deviations from the external navigation module. The figure shows that the initial phase deviation between the two 1pps signals was 266 ms, and after correction, the phase of the rubidium atomic clock's 1pps follows that of the last input 1pps from the navigation module (tending towards 0 in Figure 4). Of course, as shown in Figure 3, this initial phase also has a relatively large error and requires joint correction of time phase and frequency to gradually achieve stability. The time phase locking process is shown in Figure 5. The initial error was around 30 ns, and after approximately 1000 test points, which corresponds to 2000 seconds, the output 1pps signal stabilizes, completing the frequency and phase locking process.

Figure 4: Initial Time Phase Correction Process

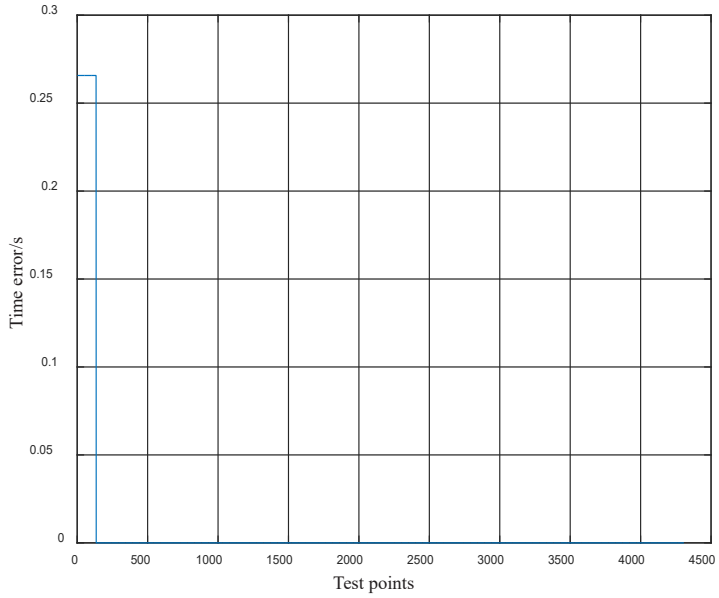
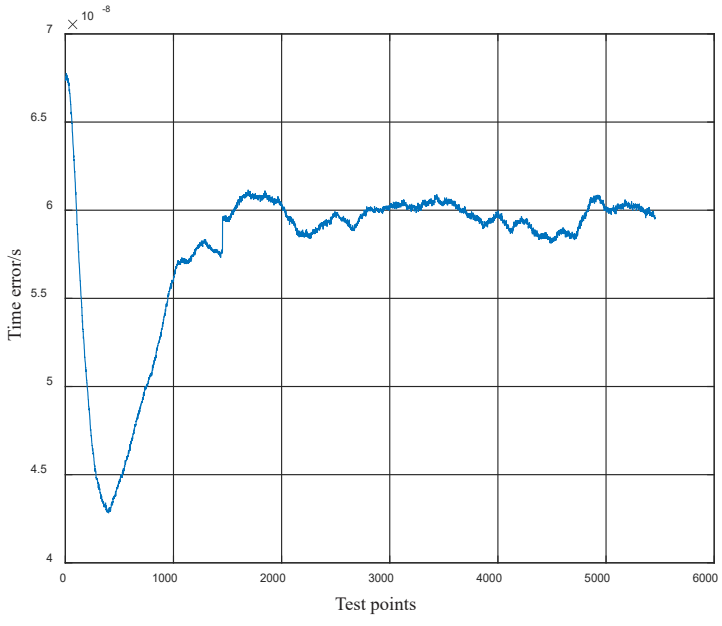


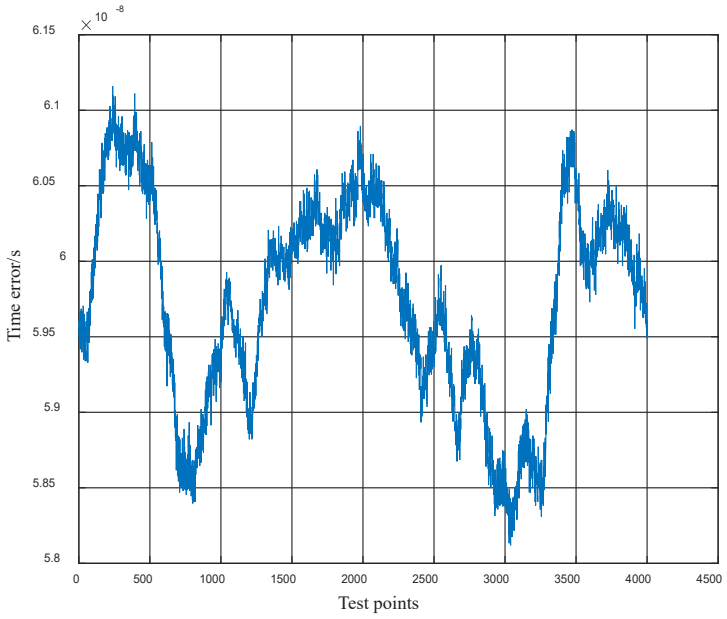
Figure 5: Time Phase Locking Process



3.3 Performance Test of 1pps After Time and Frequency Locking

The performance of the 1pps after time and frequency locking is shown in Figure 6. The variance of the data in the figure is 0.69 ns, and the difference between the maximum and minimum values is 3.04 ns. Compared to the original 1pps from the navigation module shown in Figure 3, the performance has been significantly improved. The frequency stability can be calculated as3.04ns/8000s=$3.8*10^{-13}$。

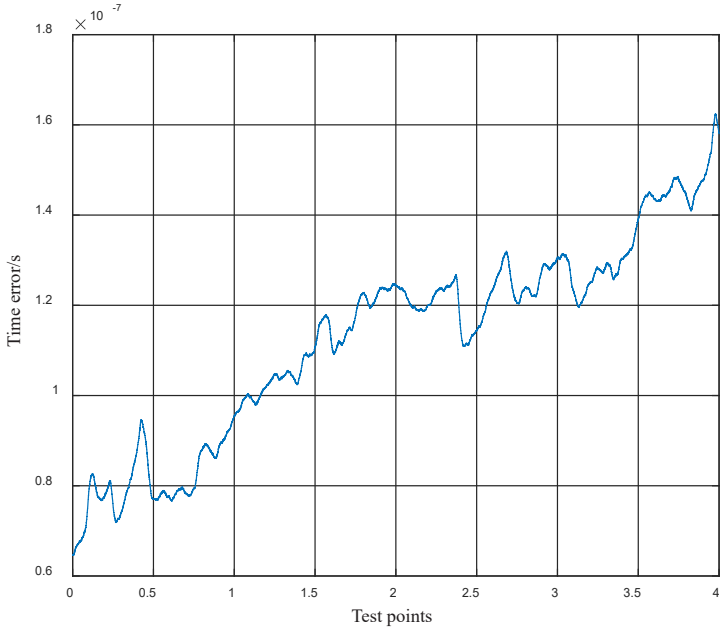
Figure 6: Performance of 1pps After Time Locking



3.4 Timekeeping Performance Test

To measure the drift after frequency locking when there is no external 1pps, a timekeeping performance test was conducted after 24 hours of locking. The test results are shown in Figure 7, with a data variance of 22.23 ns and a difference between the maximum and minimum values of 98.06 ns. This means that the error after timekeeping for 80000 seconds is about 100 ns, and the frequency error can be calculated as $1.25*10^{-12}$。

Figure 7: Timekeeping Performance After 24 Hours of Locking



4.Conclusion

Based on a second-order digital phase-locked loop, the frequency of the rubidium atomic clock is tamed using an external 1pps. Meanwhile, the loop outputs a more accurate 1pps than the external 1pps, achieving frequency and time locking

simultaneously. The algorithm is implemented using a high-speed FPGA as the processor. Test results show that both the frequency accuracy and the accuracy of the 1pps of the designed system have been significantly improved.

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no

Conflict of Interests

The author(s)declare(s) that there is no conflict of interest regarding the publication of this paper.

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